Overview on Transistor (C-MOS)

1947: first transistor

1961: first integrated circuit: 6 transistors on the same sylicon die.

With integrated circuit (IC) we mean transistors, interconnections and passive components on the same sylicon slice.

2010: i7 (INTEL): 1 Bilion of transistors with gate lenght of 32nm.

We can clearly see an hype increes of number of transistor, but why?

Because transistor can be seen as a logic switch and # of transistors is proportional to the computation capabilities.

We passed from IC with few transistors (gate lenght 100 μm) to IC with lots of transistors (Bilion) with gate lenght of 14nm.

The process of increasing number of transistors is strictly connected to the reducing their dimensions, process called SCALING.

MASTER COPY
Tel. 050 8312126
Cell. 388 9837745
050/8312126 388/9837745

Scaling

Why scaling is so important? Because

1) smaller transistors are faster $\Rightarrow$ { higher clock frequency; shorter time per operation }

2) smaller transistors need lower voltage supply $\Rightarrow$ reducing power consumption.

The idea was to follow Moore's Law and doubling number of transistor every year. But process of scaling introduced some problems, solved by working on materials:

Increasing # of transistors needs to reduce their size so: scaling process.

2003: Strained Sylicon (90nm)

The idea was to change the properties of material to improve its performances: increase mobility of electrons and holes. The process is different N-MOS (tensive - strain) and P-MOS (compressive - strain). The tensile one is realized with deposit on top of the sylicon a material with different temperature dilatation costant from its one.

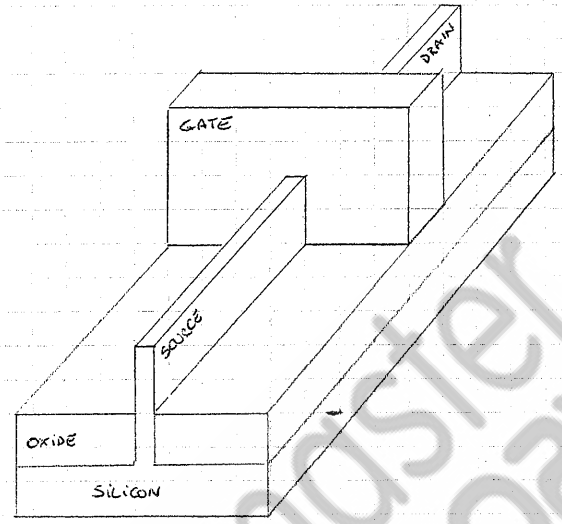
2007: Replacing Oxide (45nm)

Strained sylicon becomes a standar process, so with it was introduced another innovation that was

replace the sylicon oxide with other oxide, that reduces the tickness (of oxide) without increasing the leakage current throught the gate. On it, it's deposited directly a special combination of different metals.

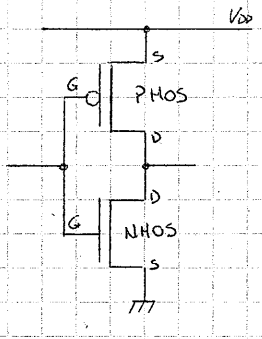
2011: Vertical transistors

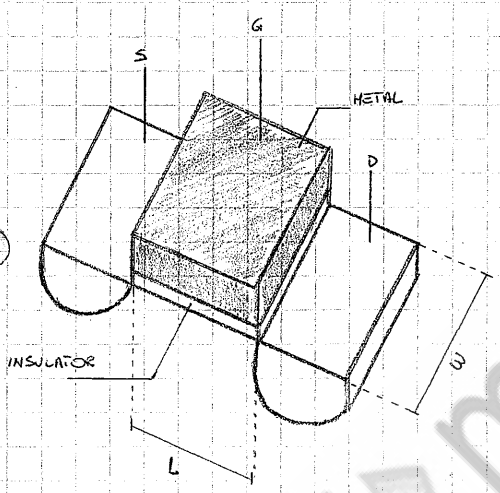
This tecnology improves electrostatic control on channel by the gate.



master COPY
MASTER COPY
Tel. 050 8312126
Cell. 388 9837745
050/8312126 388/9837745

BASIC CHOS LOGIC GATE





NHOS: 3 regions of operation (source terminal at lower voltage)

1) $V_{GS} < V_{TN}$ N OFF

2) $V_{GS} > V_{TN}$, $V_{DS} < V_{GS} - V_{TN}$ Ohmic region

$$I_D = K_n \left[(V_{GS} - V_{TN}) V_{DS} - \frac{V_{DS}^2}{2} \right]$$

The name ohmic region pathes from the fact that for small values of V_{DS}, current is almost proportional to V_{DS}:

$$I_D = K_n \left[(V_{GS} - V_{TN}) V_{DS} - \frac{V_{DS}^2}{2} \right] \approx K_n (V_{GS} - V_{TN}) V_{DS}$$

The term $(V_{GS} - V_{TN})$ is called GATE OVERDRIVE

K_n is a costan and function of material and dimension,

$$K_n = \frac{W}{L} \mu_n C_{ox}$$

- W: channel width
- L: channel lenght
- μ_n: electron mobility
- C_{ox}: dielectric capacitance of gate per unit area

$$C_{ox} = \frac{\varepsilon_0 \varepsilon_r}{T_{ox}}$$

ε_r: relative permeability of material (dielectric)

T_{ox}: oxide thickness

3) $V_{GS} > V_{TN}$ $V_{DS} > V_{GS} - V_{TN}$ Saturation Region

$$I_D = \frac{1}{2} K_n (V_{GS} - V_{TN})^2$$

Transistor behaves as an amplifier

For logic application the two most important regions are OFF (open circuit) and OHMIC (short)

PHOS: 3 region of operation (source terminal at higher voltage), $V_{TP} < 0$

1) $V_{GS} > V_{TP}$ P OFF

2) $V_{GS} < V_{TP}$, $V_{DS} > V_{GS} - V_{TP}$ ohmic region

$$I_D = K_p \left[(V_{GS} - V_{TP}) V_{DS} - \frac{V_{DS}^2}{2} \right]$$

$K_p = \frac{W}{L} \mu_p C_{ox}$, μ_p: mobility of holes

Note: $V_{DS} < 0$

3) $V_{GS} < V_{TP}$, $V_{DS} < V_{GS} - V_{TP}$ saturation region

$$I_D = \frac{K_p}{2} (V_{GS} - V_{TP})^2$$

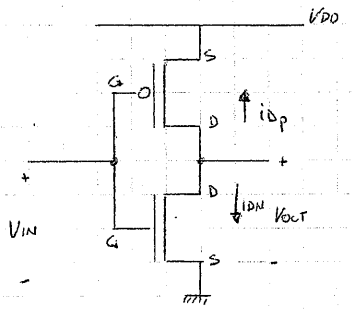
Note: $V_{DS} < 0$

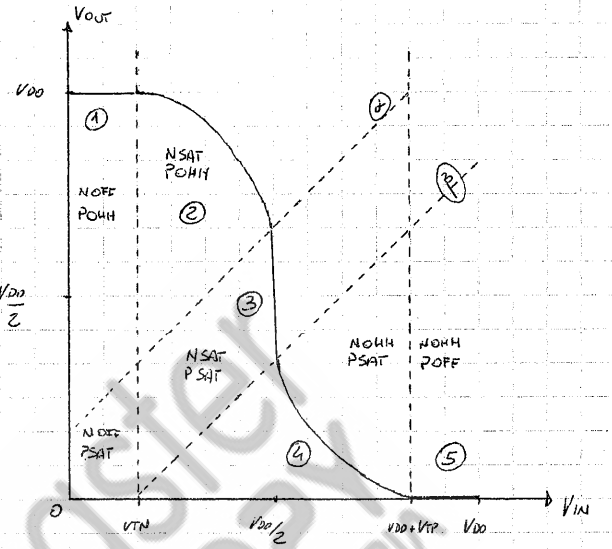
MASTER COPY
Tel. 050 831216
Cel. 388 985745
050/831216 388/985745

By knowing the voltage at terminals of transistors, we can know their working region, so value of current flowing and power consumption.

TRANSFER CHARACTERISTIC - STATIC PROPERTIES

Output voltage in function of input one





From circuit we have:

$V_{IN} = V_{GSN}$ $\quad V_{IN} - V_{DD} = V_{GSP}$

$V_{OUT} = V_{DSN}$ $\quad V_{OUT} - V_{DD} = V_{DSP}$

NMOS:

$0 \leq V_{IN} < V_{TN} \rightarrow V_{GSN} < V_{TN} \Rightarrow$ N OFF

$V_{IN} > V_{TN}$, $\begin{cases} V_{DS_N} < V_{IN} - V_{TN} \rightarrow V_O < V_{IN} - V_{TN} & \text{N ohmic} \\ V_{DS_N} > V_{IN} - V_{TN} \rightarrow V_O > V_{IN} - V_{TN} & \text{N SAT} \end{cases}$ call $V_O = V_{IN} - V_{TN}$ (β)

PMOS:

$V_{DD} + V_{TP} \leq V_{IN} < V_{DD} \rightarrow V_{GSP} > V_{TP} \Rightarrow$ P OFF

$V_{IN} < V_{DD} + V_{TP}$, $\begin{cases} V_{DSP} > V_{GSP} - V_{TP} \rightarrow V_{OUT} - V_{DD} > V_{IN} - V_{DD} - V_{TP} \rightarrow V_{OUT} > V_{IN} - V_{TP} \Rightarrow \text{P ohmic} \\ V_{DS} < V_{GSP} - V_{TP} \rightarrow V_{OUT} < V_{IN} - V_{TP} \Rightarrow \text{P SAT} \quad \text{call } V_O = V_{IN} - V_{TP} \text{ (x)} \end{cases}$

(1) when $V_{IN} < V_{TN}$ NMOS is off, so $i_D = 0A$. In this region P is in ohmic region and of cours it's current will be null at the same. So, since $i_{DP} = -K_P\left[(V_{GSP} - V_{TP})V_{DSP} - \frac{V_{DSP}^2}{2}\right] = 0 \Rightarrow V_{DSP} = 0$

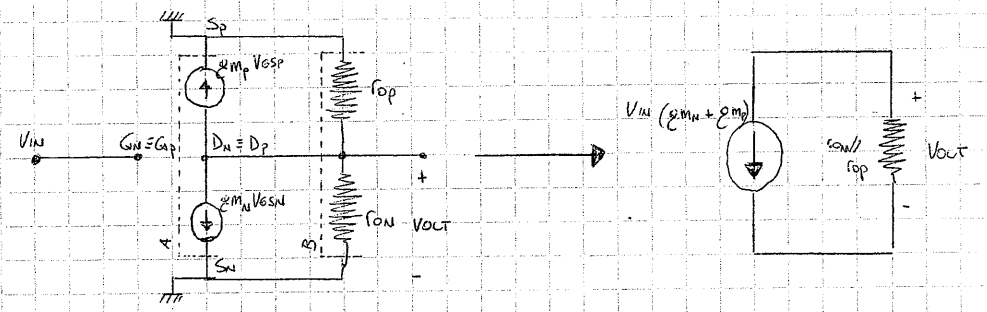
But $V_O = V_{DD} - V_{DSP}$, so $V_{OUT} = V_{DD}$

(5) When $V_{DD} + V_{TP} \leq V_{IN} < V_{DD}$, at the same, PMOS is off, so NMOS is in ohmic with a null current and this means $V_{DSN} = V_O = 0V$

(2) Starting from point (1), now NMOS is on and start to conduct and current flows baetween transistors. PMOS is still in ohmic region but, this time with $i_{DP} \neq 0A \Rightarrow V_{DSP} \neq 0V$. V_{DSP} starts to increas and since $V_O - V_{DSP} = V_{DD}$, V_O starts to decrease.

MASTER COPY
Tel. 050 8312126
Cell. 388 9837745

③ In this region both transistors are in their saturation region. Let's see what happens in a small signal equivalent:



Note that the two current generator are in parallel (A) and at the same the two resistors (B).

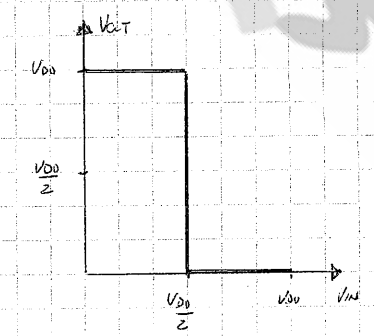
Also, $g_{mN} V_{GSN} = g_{mN} V_{IN}$, and $g_{mp} V_{GSP} = g_{mp} V_{IN}$ (should be $g_{mp}(V_{IN} - V_{DD})$, but $V_{DD} = 0V$ cause small signal).

So $V_{OUT} = -V_{IN}(g_{mN} + g_{mp})\, r_{ON} // r_{OP} \Rightarrow \frac{V_{OUT}}{V_{IN}} = -r_{ON} // r_{OP}(g_{mN} + g_{mp}) = -A_{V0}$

This value is usually very high (negative) and what obtained is the slope of the transfer function in zone 3. So, thanks to the small signal, we can say that for little variations of V_{IN}, we have by variation of Vout and this last decrease with increasing of V_{IN} (cause minus sign)

④ By increasing V_{IN} more and more V_{OUT} decreas even more and V_{DSP} increases

The characteristic obtained is not so different from the ideal one:



$$V_O = f(V_{IN}) \Rightarrow \begin{cases} V_{IN} = V_{DD} \rightarrow V_O = 0V \\ V_{IN} = 0V \rightarrow V_O = V_{DD} \end{cases}$$

Symmetric on $\frac{V_{DD}}{2}$, best noise margines!

Something like that can be obtained if characteristics of NMOS and PMOS are identical and this is if

1) $K_n = K_p$ 2) $|V_{TP}| = |V_{TN}|$

Altering V_{TN} and V_{TN} changes the regions of working and so simmetry of characteristic. The condition can be obtained by working on K_p, K_n, V_{TN} and V_{TP}. If simmetric condition is obtained, the inverter is called BALANCED INVERTER.

Condition (2) can be obtained by doping process: treating appropriately the sylicon for NMOS and PMOS

Condition (1) is obtained by geometrical consideration:

Master Copy 050/8312216 388/9837715